GigaDevice Semiconductor Inc.

GD32FFPRTGU6
Arm® Cortex®-M4 32-bit MCU

Datasheet

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1. General description

The GD32FFPRTGU6 device belongs to the specific line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. Its single precision FPU (floating point unit) speeds up software development. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32FFPRTGU6 device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 168 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1024 KB on-chip Flash memory and 128 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The device offer four general-purpose 16-bit timers, a 16-bit advanced-control timer, two 12-bit 2.6M SPS ADCs, as well as standard and advanced communication interfaces: two USARTs, two SPIs, an I2C and a USBD.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make GD32FFPRTGU6 device specifically suitable for advanced fingerprint recognition application.

2. Device overview

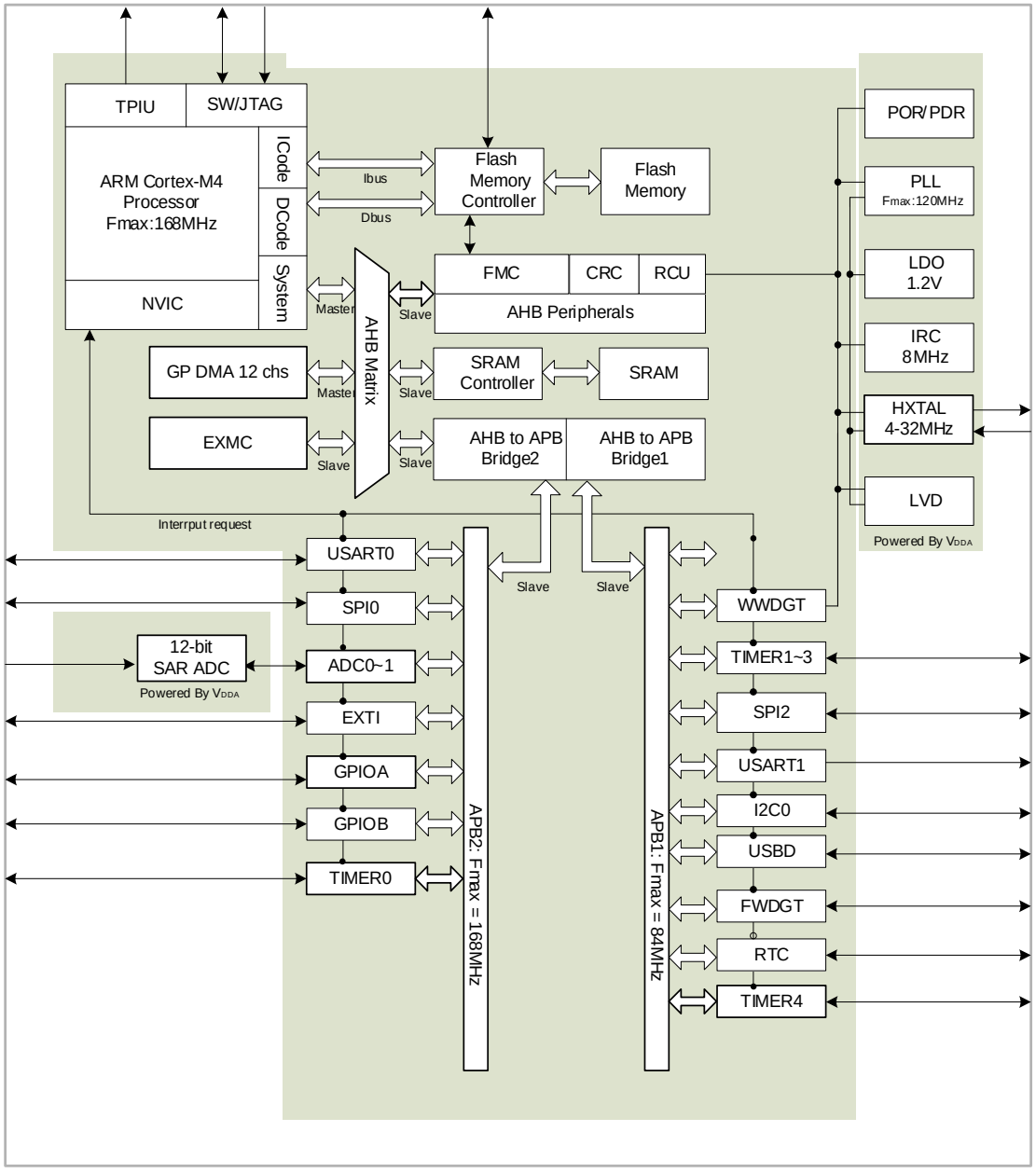
2.1. Device information

Table 2-1. GD32FFPRTGU6 device features and peripheral list

Part Number		GD32FFPRTGU6
Flash	Code Area (KB)	256
	Data Area (KB)	768
	Total (KB)	1024
SRAM (KB)		128
Timers	General timer(16-bit)	4 (1-4)
	Advanced timer(16-bit)	1 (0)
	SysTick	1
	Watchdog	2
	RTC	1
Connectivity	USART	2 (0-1)
	I2C	1 (0)
	SPI	2 (0,2)
	USBD	1
GPIO		26
EXMC		0
EXTI		16
ADC Unit (CHs)		2(10)
Package		QFN36

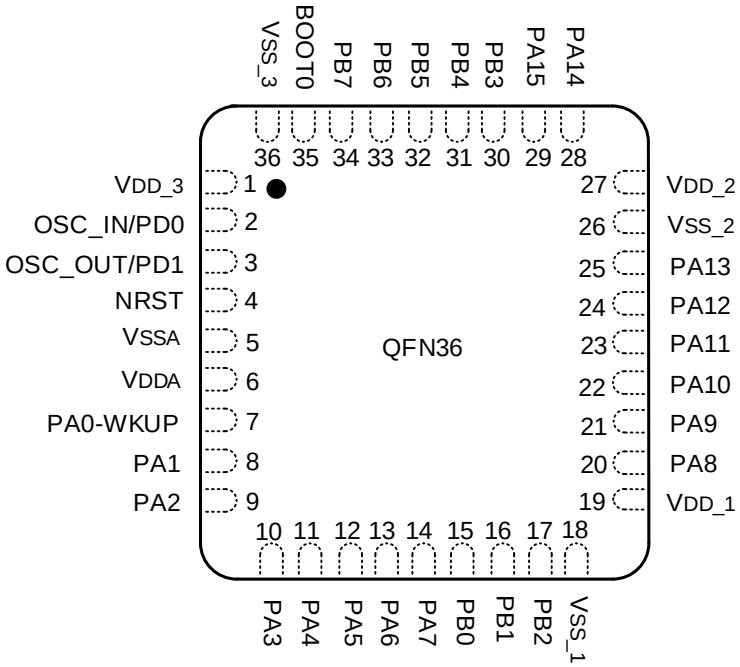
2.2. Block diagram

Figure 2-1. GD32FFPRTGU6 block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32FFPRTGU6 QFN36 pinouts



2.4. Memory map

Table 2-2. GD32FFPRTGU6 memory map

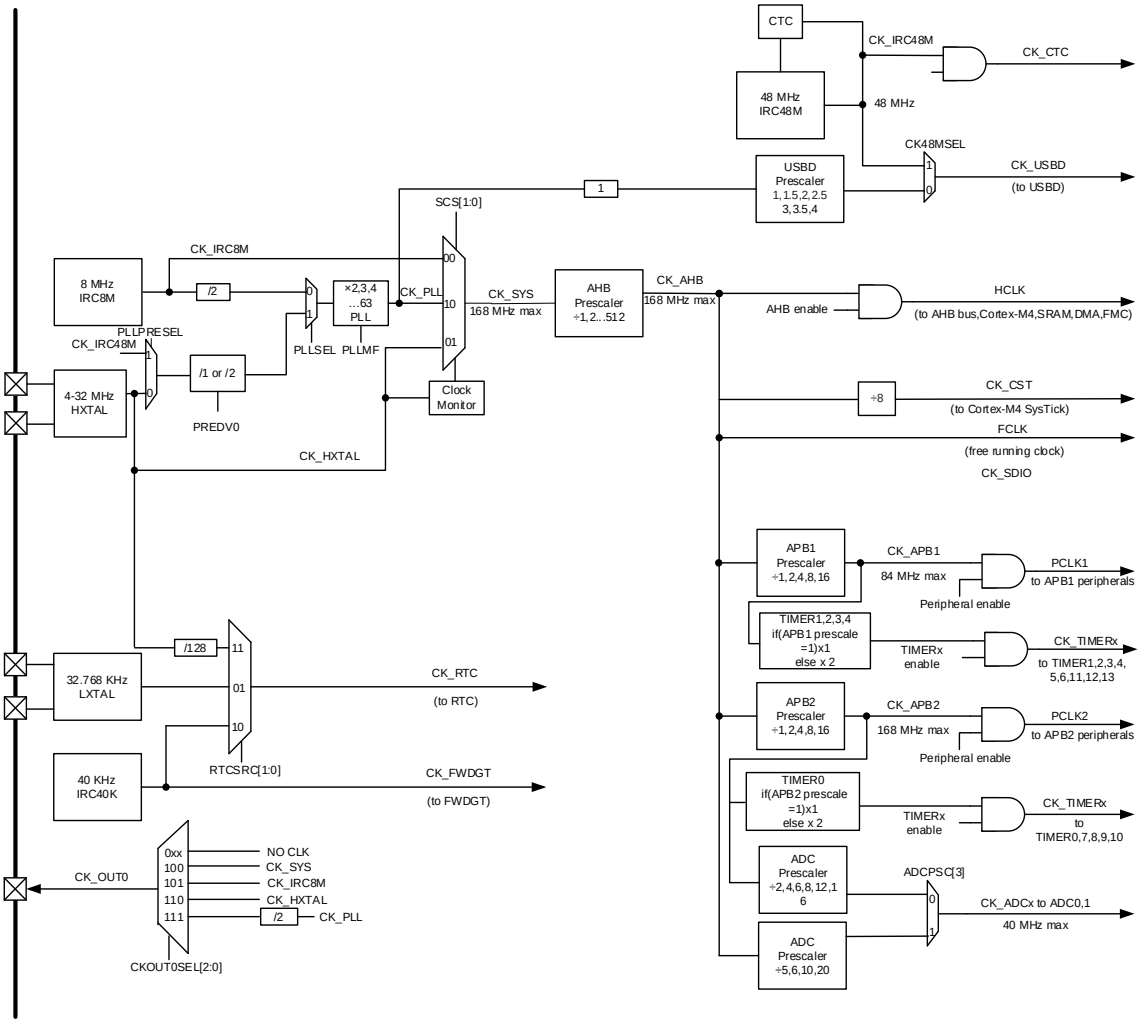
Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xA000 0000 - 0xA000 0FFF	Reserved
External RAM		0x9000 0000 - 0x9FFF FFFF	Reserved
		0x7000 0000 - 0x8FFF FFFF	Reserved
		0x6000 0000 - 0x6FFF FFFF	Reserved
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	Reserved
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	SDIO
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	Reserved
		0x4001 1000 - 0x4001 13FF	Reserved
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Shared USBD/CAN SRAM 512 bytes
		0x4000 5C00 - 0x4000 5FFF	USBD
		0x4000 5800 - 0x4000 5BFF	Reserved
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	Reserved
		0x4000 4C00 - 0x4000 4FFF	Reserved
		0x4000 4800 - 0x4000 4BFF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2
		0x4000 3800 - 0x4000 3BFF	Reserved
		0x4000 3400 - 0x4000 37FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	Reserved
		0x4000 1000 - 0x4000 13FF	Reserved
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2001 8000 - 0x2002 FFFF	Reserved
		0x2000 0000 - 0x2001 7FFF	SRAM
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF F000 - 0x1FFF F7FF	Boot loader
		0x1FFF C010 - 0x1FFF EFFF	
		0x1FFF C000 - 0x1FFF C00F	
		0x1FFF B000 - 0x1FFF BFFF	
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0800 0000 - 0x082F FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Aliased to Main Flash or Boot loader
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-3. GD32FFPRTGU6 clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8 M RC oscillators

IRC40K: Internal 40 K RC oscillator

IRC48M: Internal 48 M RC oscillators

2.6. Pin definitions

Table 2-3. GD32FFPRTGU6 pin definitions

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
OSC_IN	2	I		Default: OSC_IN
OSC_OUT	3	O		Default: OSC_OUT
NRST	4	I/O		Default: NRST
V_{SSA}	5	P		Default: V_{SSA}
V_{DDA}	6	P		Default: V_{DDA}
PA0-WKUP	7	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC012_IN0, TIMER1_CH0_ETI, TIMER4_CH0
PA1	8	I/O		Default: PA1 Alternate: USART1_RTS, ADC012_IN1, TIMER1_CH1, TIMER4_CH1
PA2	9	I/O		Default: PA2 Alternate: USART1_TX, ADC012_IN2, TIMER1_CH2, TIMER4_CH2, SPI0_IO2
PA3	10	I/O		Default: PA3 Alternate: USART1_RX, ADC012_IN3, TIMER1_CH3, TIMER4_CH3, SPI0_IO3
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 Remap:SPI2_NSS
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BKIN
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1 Remap: TIMER0_CH0_ON
PB0	15	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2 Remap: TIMER0_CH1_ON
PB1	16	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3 Remap: TIMER0_CH2_ON
PB2	17	I/O	5VT	Default: PB2, BOOT1
V_{SS_1}	18	P		Default: V_{SS_1}
V_{DD_1}	19	P		Default: V_{DD_1}
PA8	20	I/O	5VT	Default: PA8

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, CTC_SYNC
PA9	21	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1
PA10	22	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2
PA11	23	I/O	5VT	Default: PA11 Alternate: USART0_CTS, USBDM, TIMER0_CH3
PA12	24	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, USBDP
PA13	25	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
V_{SS_2}	26	P		Default: V_{SS_2}
V_{DD_2}	27	P		Default: V_{DD_2}
PA14	28	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	29	I/O	5VT	Default: JTDI Alternate: SPI2_NSS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS
PB3	30	I/O	5VT	Default: JTDO Alternate:SPI2_SCK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK
PB4	31	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	32	I/O		Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI Remap: TIMER2_CH1, SPI0_MOSI
PB6	33	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, SPI0_IO2
PB7	34	I/O	5VT	Default: PB7 Alternate: I2C0_SDA , TIMER3_CH1 Remap: USART0_RX, SPI0_IO3
BOOT0	35	I		Default: BOOT0
V_{SS_3}	36	P		Default: V_{SS_3}
V_{DD_3}	1	P		Default: V_{DD_3}

Notes:

(1)Type: I = input, O = output, P = power.

(2)I/O Level: 5VT = 5 V tolerant.

3. Functional description

3.1. Arm® Cortex®-M4 core

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive device requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core

- Up to 168 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, System bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)
- Floating Point Unit (FPU)

3.2. On-chip memory

- Up to 1024 Kbytes of Flash memory, including code Flash and data Flash
- Up to 128 KB of SRAM

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner flash at most, which includes code Flash that available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. An extra data Flash is also included for storing

data mainly. ***Table 2-2. GD32FFPRTGU6 memory map*** shows the memory of the GD32FFPRTGU6 device, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 kHz RC calibrated oscillator and external 32.768 kHz crystal oscillator
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 120 MHz The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz See ***Figure 2-3. GD32FFPRTGU6 clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PA2 and PA3). It also can be used to transfer and update the Flash memory code, the data and the vector

table sections. In default condition, boot from bank0 of Flash memory is selected. It also supports to boot from bank1 of Flash memory by setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2 V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Two 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of 12 multiplexed channels: 10 external channels, 1 channel for internal temperature sensor (V_{SENSE}), and 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: Timers, ADC, SPIs, I2C, USARTs

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8. General-purpose inputs/outputs (GPIOs)

- Up to 26 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 26 general purpose I/O pins (GPIO) in GD32FFPRTGU6, named PA0 ~ PA15 and PB0 ~ PB7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9. Timers and PWM generation

- A 16-bit advanced timer (TIMER0), four 16-bit general timers (TIMER1 ~ TIMER4)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for

output match

- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 ~ TIMER4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32FFPRTGU6 have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function

- Interrupt and wakeup event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.11. Inter-integrated circuit (I2C)

- An I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides several data transfer rates of up to 100 kHz in standard mode, up to 400 kHz in the fast mode and up to 1 MHz in the fast mode plus . The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12. Serial peripheral interface (SPI)

- Two SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Two USARTs with operating frequency up to 10.5M Bits/s

- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USARTs (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Universal serial bus full-speed device interface (USBD)

- One full-speed USB Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 8 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports device modes. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.15. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.16. Package and operation temperature

- QFN36
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings (1) (4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	—	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of QFN36	—	926	mW
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

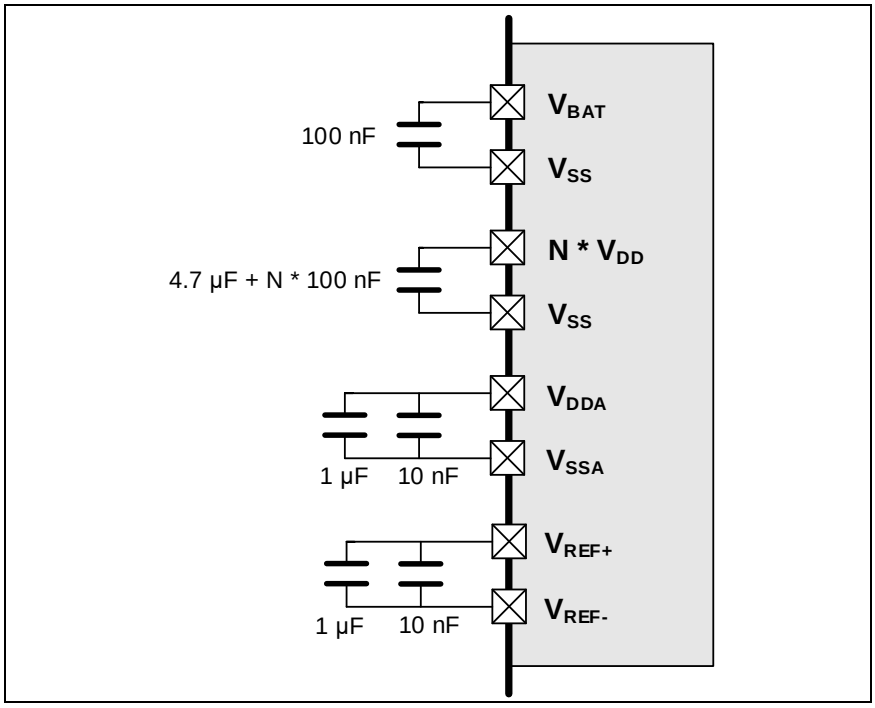
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

(1) Based on characterization, not tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) The V_{REF+} and V_{REF-} pins are only available on no less than 100-pin packages, or else the V_{REF+} and V_{REF-} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	—	—	168	MHz
f_{APB1}	APB1 clock frequency	—	—	84	MHz
f_{APB2}	APB2 clock frequency	—	—	168	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	10	ms
		Clock source from IRC8M	10	

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	3.4	µs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	5.8	
	Wakeup from Deep-sleep mode（LDO in low power mode）	5.8	

$t_{Standby}$	Wakeup from Standby mode	10	ms

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD}+I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 168 MHz, All peripherals enabled	—	35.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 168 MHz, All peripherals disabled	—	24.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, All peripherals enabled	—	26.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, All peripherals disabled	—	18.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals enabled	—	23.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals disabled	—	16.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals enabled	—	21.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals disabled	—	14.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled	—	16.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled	—	11.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	—	11.3	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	—	8.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled	—	8.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled	—	6.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	—	6.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	—	4.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	—	4.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	—	3.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	—	3.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 8 MHz, All peripherals disabled	—	2.7	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 168 MHz, CPU clock off, All peripherals enabled	—	20.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 168 MHz, CPU clock off, All peripherals disabled	—	9.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, CPU clock off, All peripherals enabled	—	15.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, CPU clock off, All peripherals disabled	—	7.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled	—	13.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, CPU clock off,	—	6.5	—	mA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		All peripherals disabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, CPU clock off, All peripherals enabled	—	12.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, CPU clock off, All peripherals disabled	—	6.0	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals enabled	—	9.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, CPU clock off, All peripherals disabled	—	4.9	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals enabled	—	7.1	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, CPU clock off, All peripherals disabled	—	3.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, CPU clock off, All peripherals enabled	—	5.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, CPU clock off, All peripherals disabled	—	3.3	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals enabled	—	4.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, CPU clock off, All peripherals disabled	—	2.8	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals enabled	—	3.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, CPU clock off, All peripherals disabled	—	2.4	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled	—	2.6	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled	—	2.0	—	mA
	Supply current	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power	—	259	—	µA

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
	(Deep-Sleep mode)	and normal driver mode, IRC40K off, RTC off, All GPIOs analog mode				
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off, All GPIOs analog mode	—	235	—	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off, All GPIOs analog mode	—	211	—	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off, All GPIOs analog mode	—	186	—	µA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, IRC40K on, RTC on	—	5.1	—	µA
		V_{DD} = V_{DDA} = 3.3 V, IRC40K on, RTC off	—	5.0	—	µA
		V_{DD} = V_{DDA} = 3.3 V, IRC40K off, RTC off	—	4.4	—	µA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, HXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

Figure 4-2. Typical supply current consumption in Run mode

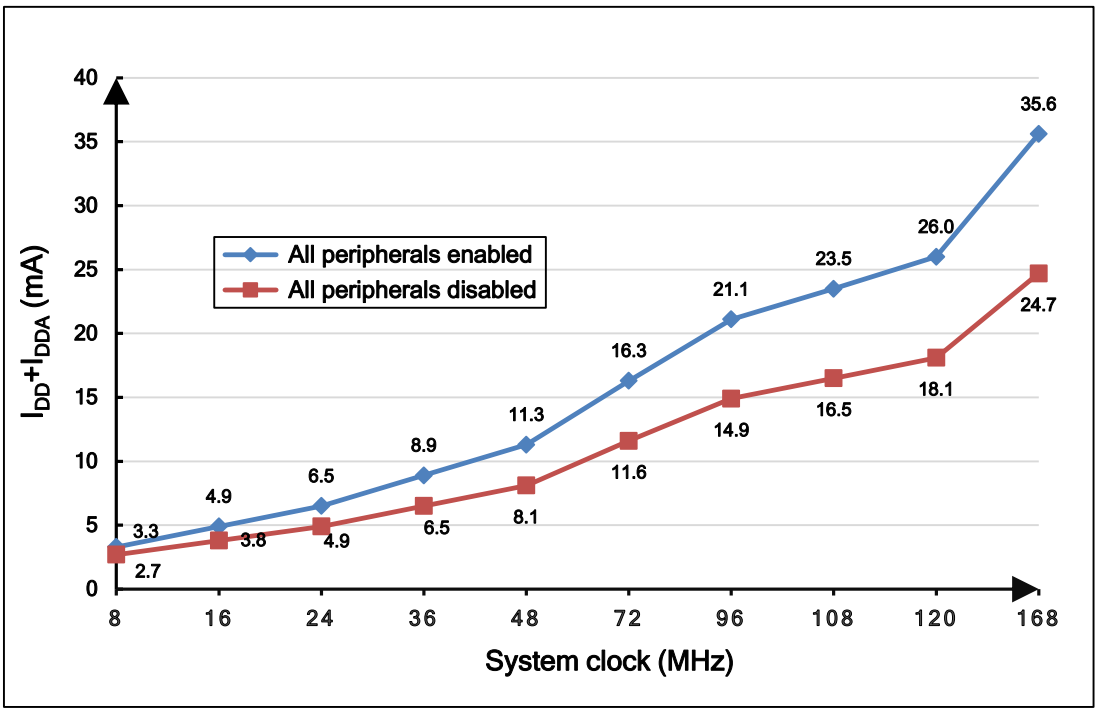
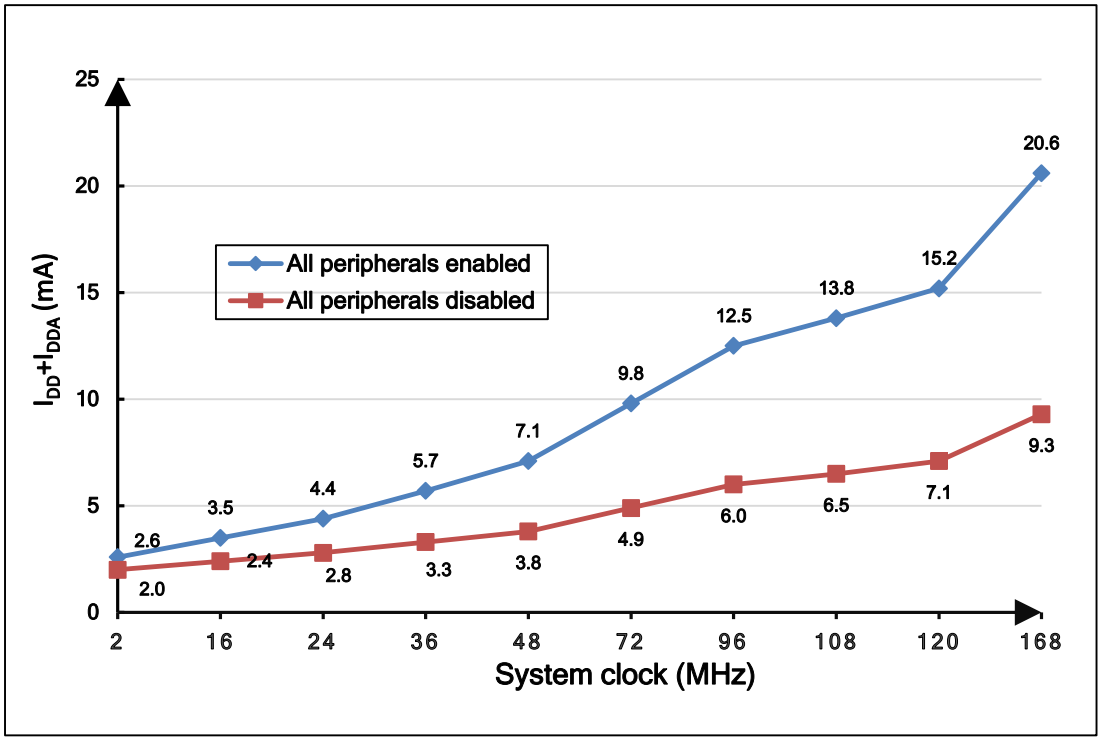


Figure 4-3. Typical supply current consumption in Sleep mode



4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-8. EMS characteristics***(1), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-8. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 168 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 168 MHz conforms to IEC 61000-4-4	4A

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	2.15	—	V

		LVDT<2:0> = 000(falling edge)	—	2.04	—	
		LVDT<2:0> = 001(rising edge)	—	2.29	—	
		LVDT<2:0> = 001(falling edge)	—	2.19	—	
		LVDT<2:0> = 010(rising edge)	—	2.43	—	
		LVDT<2:0> = 010(falling edge)	—	2.33	—	
		LVDT<2:0> = 011(rising edge)	—	2.57	—	
		LVDT<2:0> = 011(falling edge)	—	2.47	—	
		LVDT<2:0> = 100(rising edge)	—	2.71	—	
		LVDT<2:0> = 100(falling edge)	—	2.6	—	
		LVDT<2:0> = 101(rising edge)	—	2.85	—	
		LVDT<2:0> = 101(falling edge)	—	2.74	—	
		LVDT<2:0> = 110(rising edge)	—	2.99	—	
		LVDT<2:0> = 110(falling edge)	—	2.89	—	
		LVDT<2:0> = 111(rising edge)	—	3.13	—	
		LVDT<2:0> = 111(falling edge)	—	3.03	—	
$V_{LVDhyst}$(2)	LVD hystersis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	2.34	—	V
V_{PDR}(1)	Power down reset threshold		—	1.82	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	600	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	—	—	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	—	—	750	V

(1) Based on characterization, not tested in production.

Table 4-11. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(2) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.6 V ≤ V_{DD} ≤ 3.6 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DDHXTAL}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.26	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.8	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-13. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	2.6 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	40	—	60	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-14. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C(1)	—	-0.51to-0.08(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	—	66	—	µA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	—	3.6	—	µs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C	—	40	—	kHz
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz, T_A = 25 °C	—	0.4	—	µA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz, T_A = 25 °C	—	96	—	µs

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Table 4-16. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40°C ~ +85 °C(1)	—	-1.42to+0.51(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.12	—	%
$Ducy_{IRC48M}$(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	—	356	—	µA

$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 168 MHz	—	2.5	—	µs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-17. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	168	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	32	—	344	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	µs
I_{DDA}(1)(3)	Current consumption on V_{DDA}	VCO freq = 344 MHz	—	683	—	µA
$Jitter_{PLL}$(1)(4)	Cycle to cycle Jitter（rms）	System clock	—	35	—	ps
	Cycle to cycle Jitter（peak to peak）		—	371	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) Value given with main PLL running.

4.10. Memory characteristics

Table 4-18. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	100	—	—	kcycles
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A = -40°C ~ +85 °C	—	47.5	215	µs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85 °C	—	45	800	ms
$t_{MERASE(256K)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	2	24	s
$t_{MERASE(512K)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	4	48	s
$t_{MERASE(1MB)}$	Mass erase time	T_A = -40°C ~ +85 °C	—	6	72	s

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.11. NRST pin characteristics

Table 4-19. NRST pin characteristics

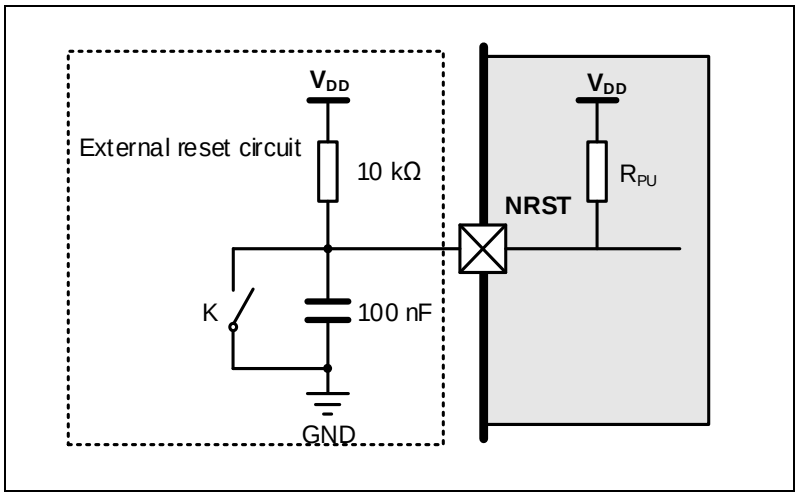
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 2.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	390	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	410	—	mV
$V_{IL(NRST)}$(1)	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	430	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-20. I/O port DC characteristics(1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8mA)	V_{DD} = 2.6 V	—	—	0.17	V
		V_{DD} = 3.3 V	—	—	0.16	
		V_{DD} = 3.6 V	—	—	0.15	
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +20mA)	V_{DD} = 2.6 V	—	—	0.49	V
		V_{DD} = 3.3 V	—	—	0.4	
		V_{DD} = 3.6 V	—	—	0.34	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8mA)	V_{DD} = 2.6 V	2.4	—	—	V
		V_{DD} = 3.3 V	3.15	—	—	
		V_{DD} = 3.6 V	3.44	—	—	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +20mA)	V_{DD} = 2.6 V	2.02	—	—	V
		V_{DD} = 3.3 V	2.8	—	—	
		V_{DD} = 3.6 V	3.15	—	—	

R_{PU}(2)	Internal pull-up resistor	All pins	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10	—	7.5	10	13.5	
R_{PD}(2)	Internal pull-down resistor	All pins	$V_{IN} = V_{DD}$	30	40	50	kΩ
		PA10	—	7.5	10	13.5	

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

4.13. ADC characteristics

Table 4-21. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{REF+}	V
V_{REF+}(2)	Positive Reference Voltage	—	2.6	—	V_{DDA}	V
V_{REF-}(2)	Negative Reference Voltage	—	—	V_{SSA}	—	V
f_{ADC}(1)	ADC clock	—	0.1	—	40	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.86	MSPS
		10-bit	0.008	—	3.33	
		8-bit	0.01	—	4	
		6-bit	0.012	—	5	
V_{AIN}(1)	Analog input voltage	16 external; 2 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	32.9	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 40 MHz	—	3.275	—	μs
t_s(2)	Sampling time	f_{ADC} = 40 MHz	0.0375	—	5.99	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-22. ADC $R_{AIN\ max}$ for f_{ADC} = 40 MHz

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.0375	0.15
7.5	0.1875	2.96

T_S (cycles)	t_S (μs)	$R_{AIN\ max}$ (kΩ)
13.5	0.3375	5.77
28.5	0.7125	12.8
41.5	1.0375	18.9
55.5	1.3875	25.4
71.5	1.7875	32.9
239.5	5.9875	N/A

Table 4-23. ADC dynamic accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25℃	—	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio		—	66.7	—	dB
SNR	Signal-to-noise ratio		—	67.4	—	
THD	Total harmonic distortion		—	-76.3	—	

(1) Based on characterization, not tested in production.

Table 4-24. ADC dynamic accuracy at f_{ADC} = 40 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 40 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 ℃	—	10	—	bits
SNDR	Signal-to-noise and distortion ratio		—	62	—	dB
SNR	Signal-to-noise ratio		—	62.2	—	
THD	Total harmonic distortion		—	-68.6	—	

(1) Based on characterization, not tested in production.

Table 4-25. ADC static accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±0.9	—	
INL	Integral linearity error		±1	—	

(1) Based on characterization, not tested in production.

4.14. Temperature sensor characteristics

Table 4-26. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.1	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.45	—	V
t_{START}	Startup time	—	—	—	μs
t_{S_temp} (2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. I2C characteristics

Table 4-27. I2C characteristics(1)(2)

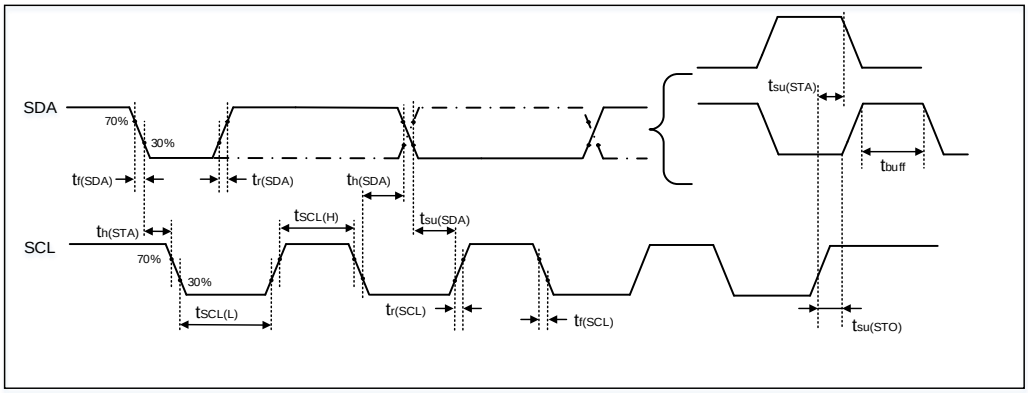
Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs

$t_{su(SDA)}$	SDA setup time	—	2	—	0.8		0.1	—	μs
$t_{h(SDA)}$	SDA data hold time	—	250	—	250	—	130	—	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	20	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs

(1) Guaranteed by design, not tested in production.

(2) Test condition :GPIO_SPEED set 2 MHz and external pull-up resistor value is 1 kΩ when operate EEPROM with I2C.

Figure 4-5. I2C bus timing diagram



4.16. SPI characteristics

Table 4-28. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 120 MHz, presc = 8	31.83	33.33	34.83	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	5	6	ns
$t_{H(MO)}$	Data output hold time	—	3	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	5	—	9	ns
$t_{DIS(SO)}$	Data output disable time	—	6	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	10	12	ns
$t_{H(SO)}$	Data output hold time	—	8	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Based on characterization, not tested in production.

Figure 4-6. SPI timing diagram - master mode

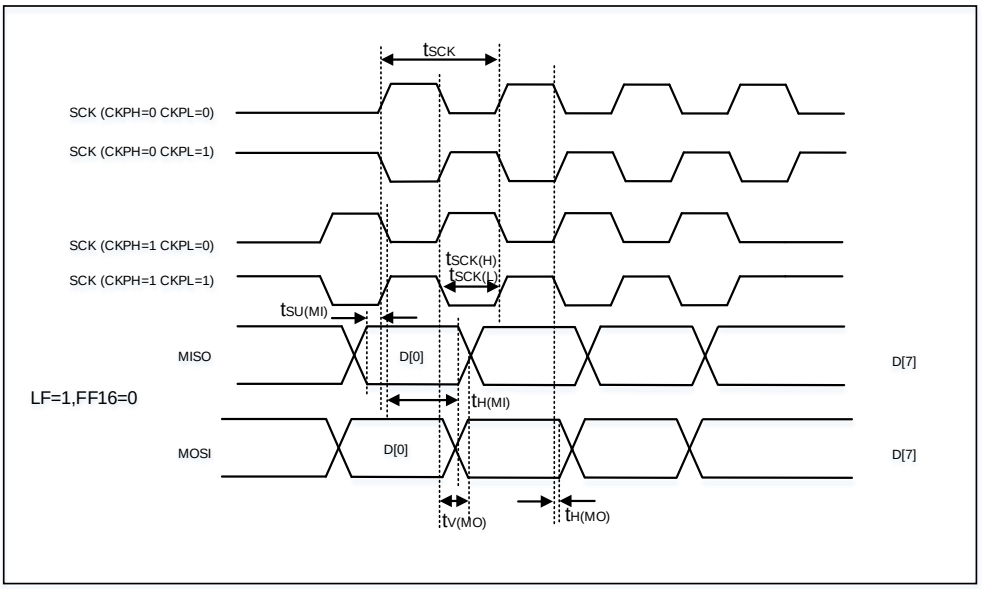
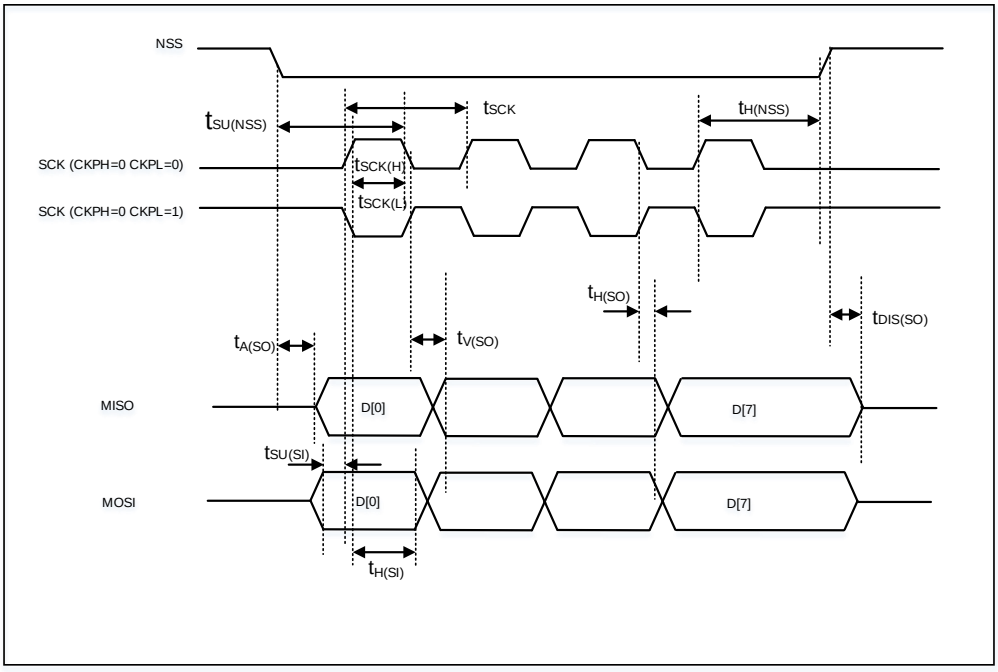


Figure 4-7. SPI timing diagram - slave mode



4.17. USART characteristics

Table 4-29. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 168 MHz	—	—	84	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 168 MHz	5.8	—	—	ns

$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 168 MHz	5.8	—	—	ns

(1) Guaranteed by design, not tested in production.

4.18. USBD characteristics

Table 4-30. USBD start up time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USBD startup time	1	μs

(1) Guaranteed by design, not tested in production.

Table 4-31. USBD DC electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels(1)	V_{DD}	USBD operating voltage	—	3	—	3.6	V
	V_{DI}	Differential input sensitivity	I(USBDP, USBDM)	0.2	—	—	V
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	1.3	—	2.0	
Output levels(2)	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V	—	0.064	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	

(1) Guaranteed by design, not tested in production.

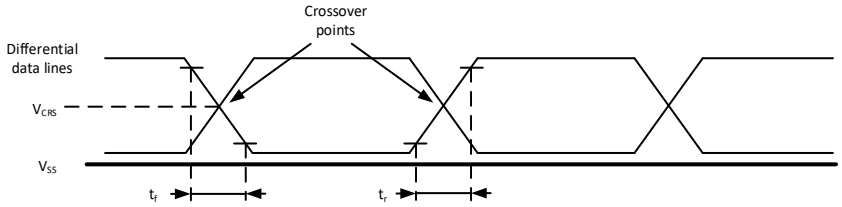
(2) Based on characterization, not tested in production.

Table 4-32. USBD full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise / fall time matching	t_R / t_F	90	—	110	%
v_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Guaranteed by design, not tested in production.

Figure 4-8. USBD timings: definition of data signal rise and fall time



4.19. TIMER characteristics

Table 4-33. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	6	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 168 MHz	0	84	MHz

RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	0.006	393	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 168 MHz	—	25.8	s

(1) Guaranteed by design, not tested in production.

4.20. WDGT characteristics

Table 4-34. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.025	409.525	ms
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

(1) Guaranteed by design, not tested in production.

Table 4-35. WWDGT min-max timeout value at 84 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	48.76	μs	3.12	ms
1/2	01	97.52		6.24	
1/4	10	195.04		12.48	
1/8	11	390.08		24.96	

(1) Guaranteed by design, not tested in production.

4.21. Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

5. Package information

5.1. QFN36 package outline dimensions

Figure 5-1. QFN36 package outline

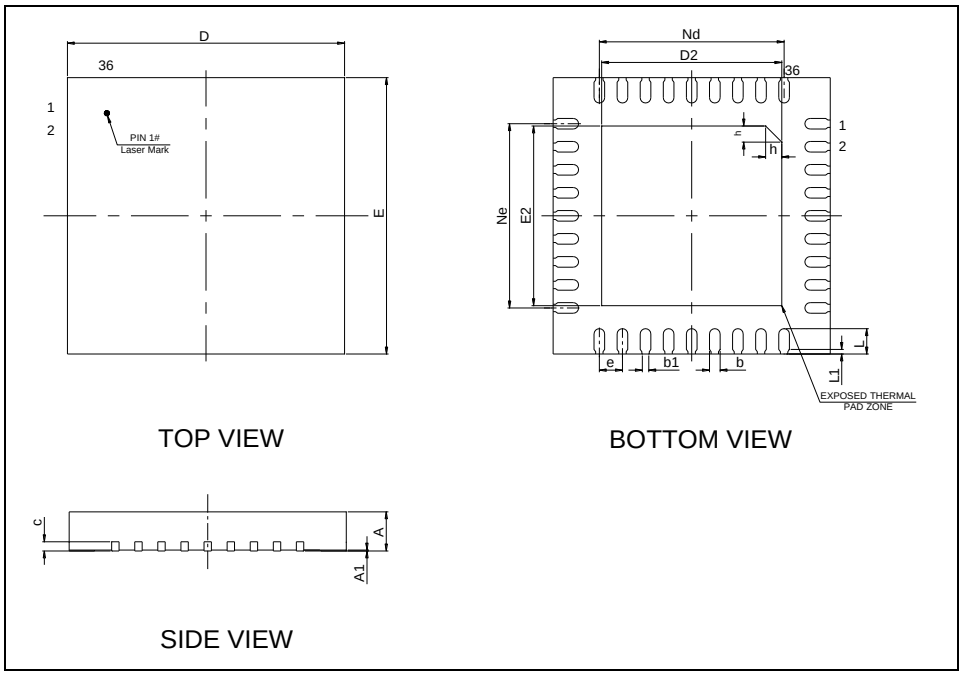
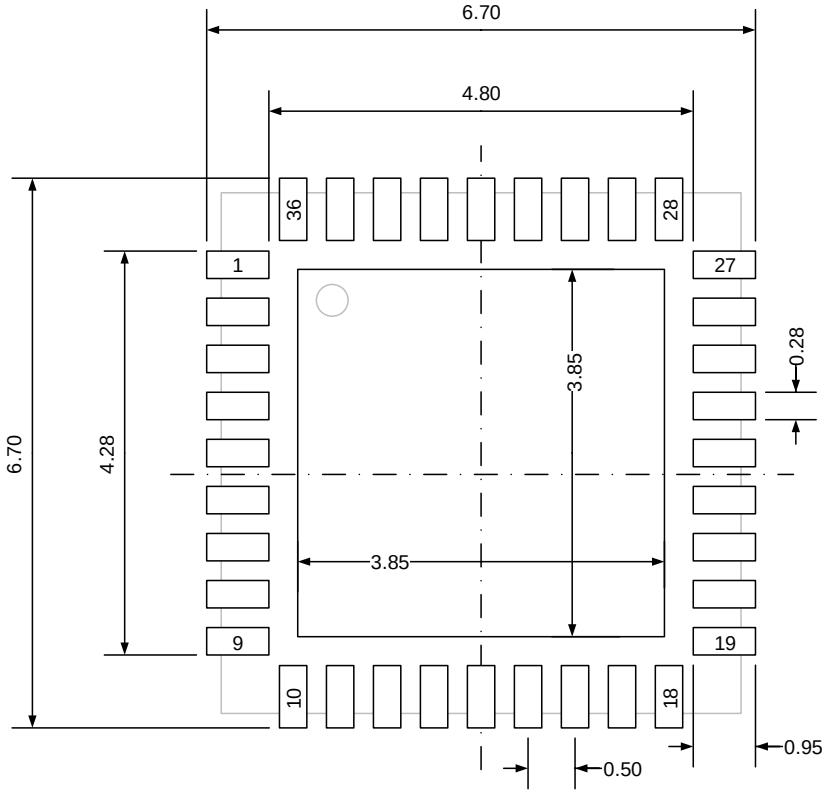


Table 5-1. QFN36 package dimensions

Symbol	Min	Typ	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.23	0.30
b1	—	0.16	—
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	3.80	3.90	4.00
e	—	0.50	—
h	0.30	0.35	0.40
L	0.50	0.55	0.60
L1	—	0.10	—
Nd	3.95	4.00	4.05
Ne	3.95	4.00	4.05

(Original dimensions are in millimeters)

Figure 5-2. QFN36 recommended footprint



(Original dimensions are in millimeters)

5.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	QFN36	43.20	°C/W
θ_{JB}	Cold plate, 2S2P PCB	QFN36	16.51	°C/W
θ_{JC}	Cold plate, 2S2P PCB	QFN36	16.18	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN36	16.64	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN36	1.07	°C/W

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32FFPRTGU6 devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32FFPRTGU6	1024	QFN36	Green	Industrial -40 °C to +85 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Jun.6, 2017
1.1	Characteristics values updated	Jun.16, 2017
1.2	1. Modify VIN max value in ***Table 4-1. Absolute maximum ratings (1) (4)*** 2. Add Power consumption values in ***Table 4-7. Power consumption characteristics (2)(3)(4)(5)*** 3. Add typical value of LVD in ***Table 4-9. Power supply supervisor characteristics*** 4. Add NRST pin characteristics 5. Complete characteristics of digital modules	Apr.20, 2022

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